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ENCHANCING AUTOMATION AND RELIABILITY IN LAPPING AND POLISHING: SIMPLIFYING SILICON PROCESSING FOR SEMICONDUCTOR FABRICATION

Author: Mark Kennedy

OVERVIEW

In semiconductor fabrication, the lapping and polishing of silicon wafers is essential for achieving precise surface quality, flatness, and dimensional accuracy. Silicon (Si) is widely used in packaging, molding, and encapsulation for applications such as power electronics, LEDs, and telecommunications. Any surface imperfections can significantly impact the performance of semiconductor devices, making it critical to ensure that the lapping and polishing processes are optimised for high quality.

The main objectives of these processes include high material removal rates (MRR), consistent surface finishes, and minimizing sub-surface damage, total thickness variation (TTV), and surface roughness. Given the high cost of silicon, refining the lapping and polishing processes helps reduce rework and material waste.

A CLOSER LOOK AT SILICON

Silicon is a versatile material, prized for its flexibility, ease of processing, and cost-effectiveness, making it a popular choice in semiconductor applications. It is commonly used for molding, encapsulation, and die attach due to its excellent insulating properties, thermal stability, and ability to withstand harsh environmental conditions. Despite being softer than more rigid materials like silicon carbide (SiC), silicon plays a critical role in semiconductor fabrication. However, its softer nature presents challenges in precision manufacturing.

To achieve the dimensional accuracy and smooth, defect-free surfaces required for high-performance semiconductor devices, silicon requires careful lapping and polishing. These processes are crucial for removing surface imperfections, improving flatness, and ensuring that the material meets the stringent requirements of modern electronics. The delicate balance of maintaining a smooth surface without damaging the material makes the lapping and polishing steps particularly important in silicon-based wafer fabrication.

THE ROLE OF LAPPING AND POLISHING IN WAFER PRODUCTION

All wafers are subject to various common stages during production. Typically, these commence with slicing the wafer from the crystal and finish with thinning of the device through lapping and polishing techniques.

Lapping is a process that is typically performed using counter-rotating plates and an abrasive with defined grain size distribution. The object of lapping is to improve the flatness and micro-roughness of the wafers.

The final material removal step in manufacturing wafers is CMP (chemical mechanical polishing), a process that allows users to generate a super-flat, mirror-like surface with atomic-scale roughness. The process is typically undertaken using the rotary or orbital motion of a chemical slurry between the wafer and a polishing plate.

In both lapping and polishing, a fundamental understanding of the process is necessary to ensure a quality result. After all, there are many variables, including different slurries and polishing pads, while parameters such as polishing rate, pressure and uniformity can all impact the surface of the wafer if they are not applied correctly.

LAW AND ORDER

To accurately predict the amount of material removed from a sample in a given time, Preston's law needs to be applied. In fact, it is possible to analyse the Prestonian behaviour of MRR to confirm process stability.

According to Preston's equation, MRR is proportional to the product of the processing pressure/load/down-force and plate velocity. In the CMP process, the polishing rate and precision are impacted not only by the slurry flow and the characteristics of the polishing plate, but also by factors such as the mechanical action between the wafer and the plate, the chemical action resulting from the chemical components of the slurry, and the interactions between them. In short, timers based upon predictions from Preston's law can be used to accurately predict the amount of material removed from a sample.

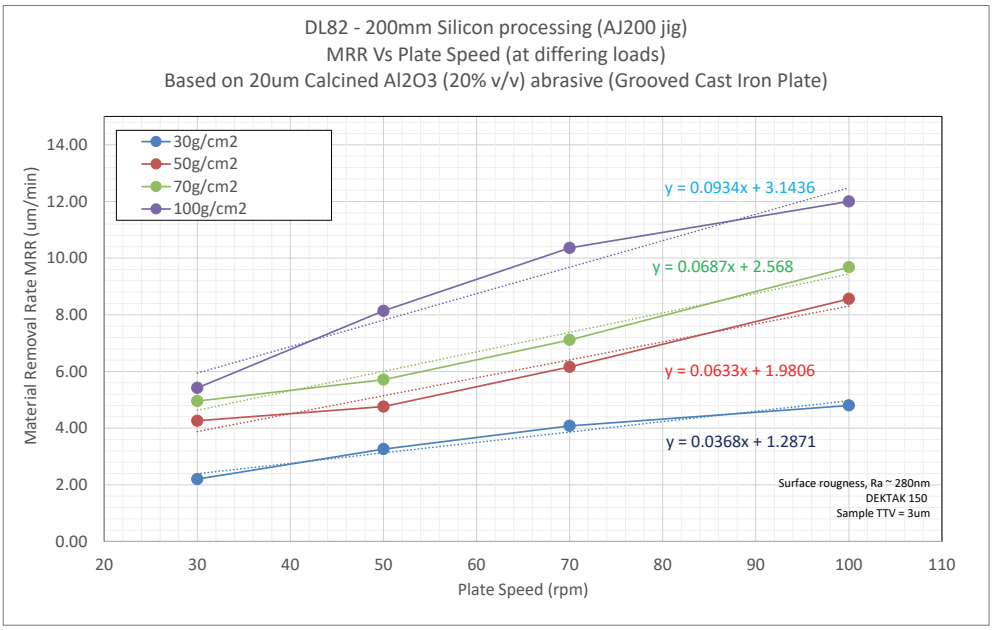
It almost goes without saying that achieving the precision and surface finish required in hard wafer applications is a skilled job. This is due chiefly to the levels of manual set- up and control needed. The process is also laborious and not conducive to the high levels of throughput demanded by industry. After all, the quest for cost reductions in the manufacture of semiconductor devices are driven by volume and yield.

Enhancing Automation and Reliability in Lapping and Polishing: Simplifying Silicon Processing for Semiconductor Fabrication

PROCESS DATA ANAYSIS: SILICON LAPPING WITH THE DL82 SYSTEM

Trials involving the lapping of 200mm Silicon Wafer showed impressive results. Using 20µm Calcined AI203 (20% v/v) abrasive and a radial grooved cast iron plate across the Material Removal rate was assessed across the plate speed range of 30rpm - 100rpm and loading groups of 30 - 100g/cm2 (equivalent of 9.5kg to 31.5kg load for a 200mm diameter wafer).

Silicon Lapping with Calcined AI203



For a pressure of 100g/cm2

MRR = 0.00093(P*V)+3.144

For a pressure of 70g/cm2

MRR = 0.00098(P*V)+2.568

For a pressure of 50g/cm2

MRR = 0.00127(P*V)+1.981

For a pressure of 30g/cm2

MRR = 0.00122(P*V)+1.287

The results show good Material Removal Rate (MRR) Vs Plate Speed linearity across each loading group, which leads to good predictable processing relationships.

KEY FEATURES AND BENEFITS

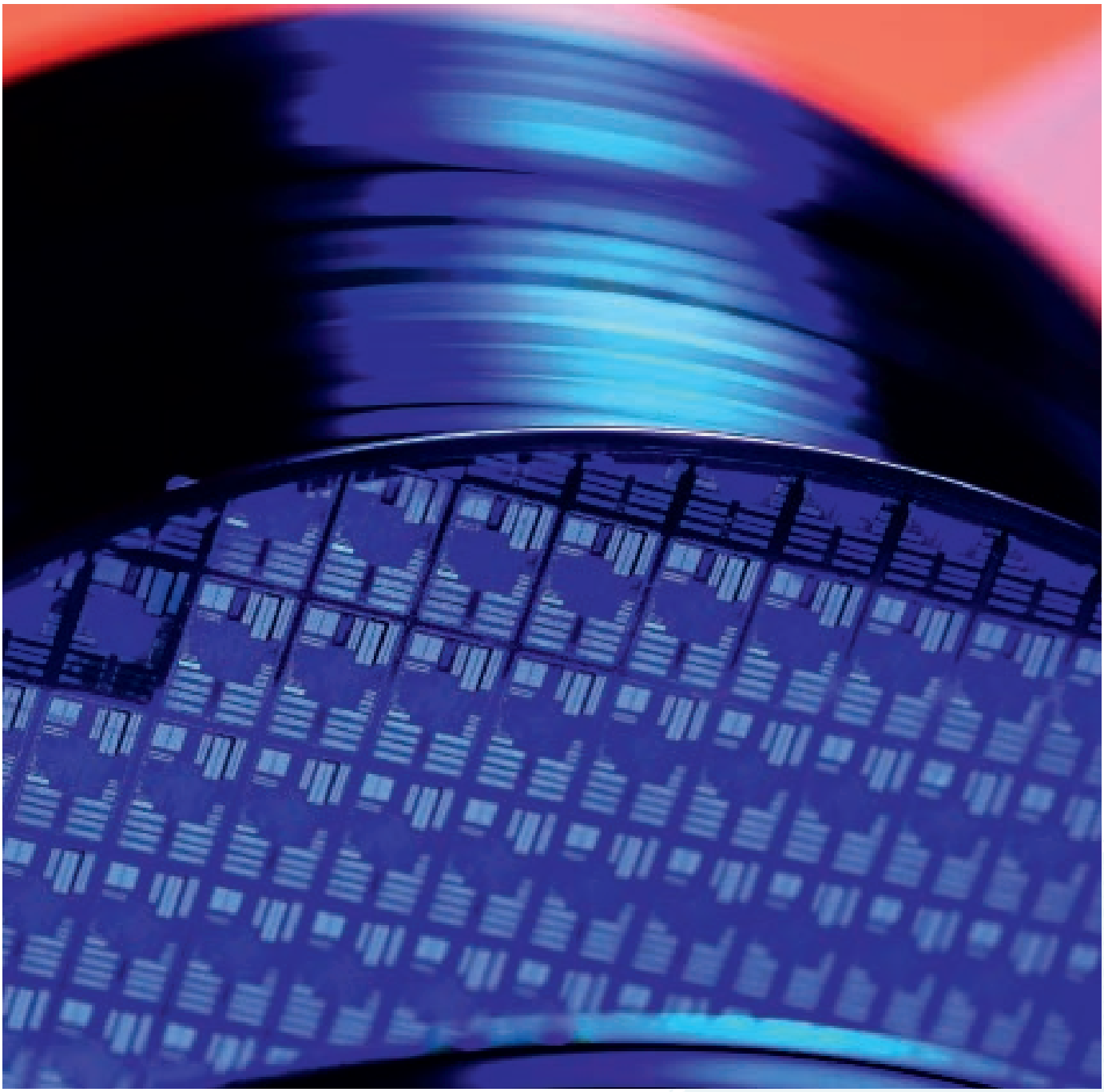
Available in two configurations: the DL82 option, which features two automatic workstations, and the DL81, which includes one automatic and one manual workstation.

The DL81 and DL82 high-precision lapping and polishing systems offer advanced automation for processing silicon wafers with exceptional precision and efficiency. With flexible configurations - one automatic and one manual station for the DL81, and two automatic stations for the DL82 - these systems can handle large 700 mm plates and various wafer sizes, ensuring optimal processing of up to 12" (300 mm) free lapped or 8" (200 mm) jig-held samples. Automated jig handling with adjustable air jigs, in-situ load cell calibration, and a metered abrasive feed system (5-100 ml/min) minimize manual intervention, enhance repeatability, and improve processing precision. The multi-stage lapping/ polishing process is efficiently supported by four 3.8 L cylinders, with a sealed system for safe hazardous material handling.

Additionally, the DL81 and DL82 systems feature smart control and monitoring capabilities, including a 15" touch screen, real-time thickness feedback, Bluetooth flatness control, and automated diagnostics via EtherCAT, ensuring consistent results and reducing human error. Recipe mode allows for repeatable operations, and the traffic light status tower provides real-time process oversight. Automation of these critical processes leads to higher throughput, reduced labor costs, and improved yield, making the DL81 and DL82 ideal for high-volume, high-precision silicon wafer processing in semiconductor manufacturing.

CONCLUSION

Lapping and polishing are critical processes in semiconductor fabrication, particularly for ensuring the precision, surface quality, and dimensional accuracy of silicon wafers. The optimisation of these processes, including the application of Preston's law for material removal prediction, is essential for improving performance, reducing waste, and meeting the stringent requirements of modern electronics. Advanced systems like the DL81 and DL82 offer significant advantages through automation, enhancing efficiency, repeatability, and throughput while minimising manual intervention. These innovations support the growing demand for high-precision, high-volume production, ultimately improving yield and reducing labor costs in semiconductor manufacturing.



LOGITECH
Materials Technologists & Engineers

LOGITECH LTD
Erskine Ferry Road
Old Kilpatrick
Glasgow, G60 5EU
United Kingdom

Tel: +44 (0) 1389 875 444

Email: enquiries@logitech.uk.com

Web: logitech.uk.com